**Computer Architecture  
CSCE 3301-01  
Fall 2019  
MS1 Journal – Marwan Eid  
October 28th, 2019  
For  
Dr. Cherif Salama**

* November - 15th – 5:30 pm : 7:45 pm: Met with Abdelhakim and Mohammed after reading the support files of the project to discuss it and discuss how we are going to work.
* November - 17th – 4:00 pm : 12:00 am: Together with Abdelhakim, implemented and simulated the pipelined processor working properly with the single ported memory
* November 18th – 1:00 pm : 4:30 pm: Modified few things in the Verilog modules; added comments to all modules; edited modules to follow coding guidelines.
* November 19th – 7:00 pm : 4:00 am: Together with Mohammed implemented and simulated the bonus compression module and integrated it in the datapath.